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The CRISP Microprocessor: Collected Papers

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ABSTRACT

This is a reconstruction of CSTR #138, based on versions of papers found on disks, except for 'An Analysis of C Machine Support for Other Block-Structured Languages', for which we can find no source, and 'Register Allocation for Free: the C Machine Stack Cache', which was scanned.

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Introduction and Overview

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Since its inception, the Computing Science Research Center has maintained an active interest in systems architecture and hardware design. In the mid-1970's interest arose in building a processor optimized towards the fast execution of programs written in the C programming language. A number of designs for C-machines were proposed and built between 1975 and 1980, but it was not until 1981 that the architecture to be used in CRISP was selected. Preliminary studies suggested that an order of magnitude improvement in performance over popular minicomputers of the time would be possible. Although the architecture was well suited for ECL implementation, rapid advances in the scale of VLSI made a single-chip microprocessor feasible as well. In early 1983 an informally organized design team was gathered for a CMOS single-chip implementation, which was given the name CRISP. The design team included members from several different organizations and locations within Bell Laboratories and had a range of skills that included computer architecture, logic design, circuit design, VLSI layout, device physics, and CAD.

In February of 1986 the first set of masks was submitted for fabrication using AT&T's 1.75 micron twin-tub CMOS process. The chip contained 172,163 actual transistors on a die that was 10.35 mm x 12.23 mm. Working silicon was obtained in the summer of 1986. This first silicon, which ran at a clock rate of 16MHz, performed significantly better than the design's target rate of 10Mhz. Of course, clock rates alone are not a particularly meaningful measure of chip performance. A much better measure is provided by one of the standard benchmarks like the Dhrystone program. The attached table lists this figure of merit for many popular processors as well as several versions of CRISP. Mask 2 of CRISP was submitted for fabrication in November of 1986 and contains several performance enhancements as well as a few minor architecural changes. It is expected to run at 20 Mhz.

This document contains a series of papers that explain the major architectural and implementation innovations in CRISP. They are presented in historical order, beginning with Ditzel and McLellan's paper ''Register Allocation for Free: the C Machine Stack Cache.'' This paper, whose appearance roughly coincided with commencment of the CMOS implementation effort, presents several of the key ideas underlying CRISP. A key methodological idea is that careful measurements and simulations performed at the onset of a design allow both architects and implementers to quickly discover which portions of the design most critically affect performance. A key architectural idea is that a stack cache used instead of explicit registers simplifies compilation and decreases the overhead associated with procedure calls. The stack cache allows

MACHINE TYPE	PROCESSOR	OPERATING SYSTEM	COMPILER	DHRYSTONES/SEC.	
				NO REG	REGS
Commodore 64	6510-1MHz	C64 ROM	C Power 2.8	36	36
IBM PC	8088, 4.77mhz	PC-DOS 2.1	Aztec C v3.2d	423	454
Macintosh	68000-7.7MHz	-	MegaMax C 2.0	661	709
ATT 3B2/300	WE32000	UNIX 5.0.2	cc	735	806
Macintosh	68000-7.8MHz	Mac Rom	Mac C 16 bit int	877	909
AT&T 6300	8086, 8mhz	MS-DOS 2.11	Aztec C v3.2d	862	943
IBM PC/XT	8086-9.54MHz	PCDOS 3.1	Lattice 2.15	980	980
VAX 11/750	w/FPA	UNIX 4.3bsd	cc	994	997
ATT PC7300	68010-10MHz	UNIX 5.2	cc	1041	1111
Sun2/120	68010-10MHz	Sun 4.2BSD	cc	1136	1219
PDP 11/70	-	UNIX 5.2	cc	1162	1250
Sun2/120	68010-10MHz	Standalone	cc	1219	1315
ATT 3B2/400	WE32100	UNIX 5.2	cc	1315	1315
ATT PC6300+	80286-6MHz	MSDOS 3.1	CI-C86 2.20M	1428	1428
IBM PC/AT	80286-7.5MHz	Venix/286 SVR2	cc	1333	1449
VAX 11/780	-	UNIX 5.2	cc	1515	1562
MicroVAX-II	-	-	-	1562	1612
VAX 11/780	-	UNIX 4.3bsd	cc	1646	1662
ATT 3B20	-	UNIX 5.2	cc	1515	1724
IBM PC/STD	80286-8MHz	MSDOS 3.0	Microsoft 3.0	1724	1785
DEC-2065	KL10-Model B	TOPS-20 6.1	Port. C Comp.	1937	1946
DEC2060	KL-10	TOPS-20	cc	2000	2000
IBM-4341-II	-	VM/SP3	Waterloo C 1.2	3333	3333
SUN 3/75	68020-16.67MHz	SUN 4.2 V3	cc	3333	3571
IBM-4341	Model 12	UTS 5.0		3685	3685
SUN-3/160	68020-16.67MHz	Sun 4.2 V3.0A	cc	3381	3764
Sun 3/180	68020-16.67MHz	Sun 4.2	cc	3333	3846
IBM-4341	Model 12	UTS 5.0		3910	3910
VAX 8600	-	UNIX 4.3bsd	cc	7024	7088
AT&T CRISP	***10MHz Mask 1***		***AT&T Research***	***8200***	***8200***
AT&T CRISP	***10MHz Mask 1***		***AT&T Summit***	***8475***	***8475***
MIPS Co	8 MHz	UMIPS BSD 1.0	cc -01	8855	10309
CRAY-XMP/12	105MHz	COS 1.14	Cray C	10204	10204
AT&T CRISP	***16MHz Mask 1***		***AT&T Summit***	***13560***	***13560***
CRAY-1A	80MHz	CTSS	Cray C 2.0	12100	13888
IBM-3083	-	VM/CMS HPO	Waterloo C 1.2	13889	13889
Amdahl 470 V/8	-	UTS/V 5.2	cc v1.23	15560	15560
CRAY-XMP/48	105MHz	CTSS	Cray C 2.0	15625	17857
IBM-3083	-	UTS 5.0 Rel 1	cc	16666	12500
AT&T CRISP	***20MHz Mask 2***		***AT&T Summit***	***16950***	***16950***
Amdahl 580	-	UTS 5.0 Rel 1.2	cc v1.5	23076	23076
Amdahl 5860	-	UTS/V 5.2	cc v1.23	28970	28970

Table: Dhrystone Benchmark Figure for Various Processors.

technological flexibility because its size is a property of the implementation, not the architecture. The 1983 paper by Hill entitled ‘‘An Analysis of C Machine Support for Other Block-Structured Languages’’ shows that C programs are not the sole beneficiaries of the CRISP architecture; many other languages enjoy greatly enhanced performance as well. The CAD tools used to build CRISP are described in ‘‘Experience with CAD Tools for a 32-Bit VLSI Microprocessor.’’ The paper ‘‘A Pipelined 32b Microprocessor with 13Kb of Cache Memory’’ gives a description of some of the physical details of the chip along with the earliest performance measurements made on actual silicon.

This is followed by a group of three papers from the Spring 1987 COMPCON conference. ‘‘Introduction to the CRISP Instruction Set Architecture’’ describes the chip from the viewpoint of the assembly language programmer. ‘‘Architectural Innovations in the CRISP Microprocessor’’ introduces the notion of branch folding and describes how pipelining is used in CRISP. ‘‘Compiling for the CRISP Microprocessor’’ describes a number of ways in which a compiler can exploit the architecture of CRISP to achieve greater execution efficencies. A key point here is that the various optimizations described are not necessary for correct execution of object programs but are done purely to enhance performance. Unlike many other state-of-the-art microprocessors, CRISP can be used successfully by very simple compilers.

The final two papers, presented at the 14th Annual Symposium on Computer Architecture, go into still greater detail concerning the implementation. ‘‘The Hardware Architecture of the CRISP Microprocessor’’ goes into a structural description of the chip and explains the function of the major components and pipeline stages. ‘‘Branch Folding in the CRISP Microprocessor: Reducing Branch Delay to Zero’’ discusses the decoded instruction cache and explains how branch instructions are effectively removed from the instruction stream by doubling them up with adjacent instructions. This process is done in such a way as to minimize delays in the instruction execution pipeline.

A great many people contributed in a great many ways to the successful fabrication of the research prototype of CRISP. The key architects and implementers included Dave Ditzel, Rae McLellan, Alan Berenbaum, Bob Cmelik, Brian Colbry, Don Freeman, Fred Heaton, George Janac, Kerry Maletsky, Kevin O’Connor, and Masakazu Shoji. They were helped by a host of colleagues that made contributions ranging from brief consultations through several months of effort. Although the following list is probably incomplete, the CRISP team is grateful for the assistance provided by Bryan Ackland, Pramad Agrawal, Jeff Arnold, Jim Arnold, Sumit Bandhyaypady, Vimal Begwani, Tung Chang, Duc Chau, Jorge Cruz-Rios, Carl Ebling, Chris Fairchild, Rob Franzo, Kevin Grant, Alan Greenberger, Mike Harmon, Dave Inglis, Merril Isenman, Steve Johnson, Milan Jukl, Paul Kollaritch, Dave Krystal, Pamela Kumar, Charles Lee, Joe Lee, Bill Metcalfe, Ken Mninich, Dave Murphy, Rob Murray, Bob Pajak, Rich Piepho, Fred Remite, Walter Roper, Marty Saniski, Harry Schonberger, Bruce Swinyer, Tom Szymanski, Ken Thompson, Ron Wadsack, Neil Weste, Chris Van Wyk, and Mike Zalonis. The implementation effort was supported by many managers within AT&T including Glen Cheney, Sandy Fraser, Lee Gallagher, Ellen Hedrick, Victor Huang, Howie Jacobs, Mike Killian, Ed Kozemchek, Priscilla Lu, Jack Molinelli, Joe Nahas, Arno Penzias,

Summit Roy, Bob Scavuzzo, Dave Thompson, Vic Vyssotsky, and Peter Weinberger. The timely fabrication of the chip was due to the fine efforts of the people at the AT&T production facilities in Allentown, Pennsylvania.