VLSI Design and Test Workshops 2001
Advance Program

(http://vlsi_india.tripod.com/vdat01/adpgm.html)

August 16-18, 2001
Bangalore, India

Scope: To promote applications and research related to all aspects of VLSI
In Cooperation With: *VLSI Society of India, IEEE Computer Society Technical Council on Test Technology*
With Support From: *Cypress Semiconductors, India; ControlNet, India; Indian Institute of Technology, Delhi; Philips Semiconductors, India; Texas Instruments, India.*

Venue: **JN Tata Auditorium, Indian Institute of Science, Bangalore, 560012**
Click to see the Registration Form

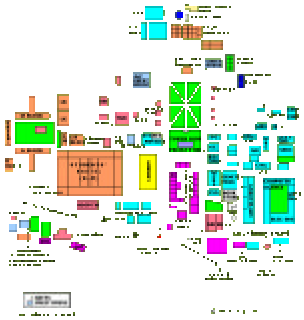
Advance Program for August 17, 2001 (Friday)

Time	***Test Workshop Chair: C.P. Ravikumar Room: A***	***High Level and Logic Design Workshop Chair: Anshul Kumar Room: Main Auditorium***	***Physical Design and VLSI Technology Workshop Chair: Bhargab B. Bhattacharya Room: B***
8:00 to 9:00 AM	***Registration***		
9.00 AM-10.00 AM	Combined with L1	**Session L1: Design Closure Chair: TBA** V. Arvind, K. Sampath P.R. Suresh and **V. Visvanthan,** Texas Instruments, India. *Electrical Design Closure: A Review of the Sate-of-the-Art and Challenges. Invited Talk.*	Combined with L1
10:00 - 10:30 AM	***Tea Break***		
	Session T1: SOC Verification Chair: TBA	**Session L2: Digital Signal Processing Chair: TBA**	**Session P1: New Horizons in VLSI Technology Chair: TBA**
10:30 to 11:00 AM	**Venkatesh Natarajan,** Texas Instruments, India. *Hardware Emulation in Systems and SOC Design, Invited Talk.*	**Rajesh Pande** and Sumeet Deshpande**,** Soft Polynomials, Nagpur, India. *Implementation of finite Impulse Response (FIR) Filter on Xilinx FPGA.*	**P. Chakrabarti,** Banaras Hindu University. Optoelectronic *Integrated Circuit (OEIC) Receivers.*
11.00 to 11.30 AM		**Puneet Goel**, Motorola, Gurgaon, India. *An Area-efficient Bit-Serial FIR Filter Architecture.*	
11.30 to 12.00 Noon		**Subash Chander** and G. Ajit Gupte, Texas Instruments, India. *A methodology for Opcode Assignment to Reduce Area and Delay of Instruction.*	**S. K. Lahiri**, IIT Kharagpur. *VLSI / ULSI Device and Process Technology, Invited Talk.*
12.00 Noon to 12.30 PM		**S. Ali** and Faquir Jain**,** Univ. of Cincinnati. *Design of RF CMOS Phase-Locked Loop and Frequency Synthesizer.*	
12.30 PM to 1.30 PM	***Lunch***		

	Session T2: Formal Verification Chair: TBA	Session L3 : Embedded Systems Chair: TBA	Session P2: Design Techniques Chair: TBA
1:30 PM to 2:00 PM	**Mandayam Srivas**, Realchip, Chennai, India. *Formal Verification of VLSI Systems. Invited Tutorial.*	**M. Balakrishnan,** IIT Delhi**.** *ASSET: A Methodology for Automated Synthesis of Embedded Systems. Invited Talk.*	Andrew Marshall**, Sreedhar Natarajan**, and Homi Moghul, Texas Instruments, Dallas, USA. *Comparative Performance of Ring Oscillators on Bulk and SOI Substrates.*
2:00 to 2:30 PM			**E. Simi**, S.S. Sudheer, and Navakant Bhat, Indian Institute of Science, Bangalore. *Dual Vt Technology using Dual Thickness Gate Oxide.*
2:30 to 3:00 PM			**H. Saha,** J.Das, S.Dey, and A. Bagchi, Jadavpur University, *Development of a Smart Humidity Sensor based on Porous Silicon.*
3:00 PM to 3:30 PM			**Jonathan Oh**, Mentor Graphics, Singapore. *Physical Verification Methodology*.
3.30 PM to 4.00 PM	*Tea Break*		
	Session L4: EDA **Chair: TBA**	**Session L5: Memory Design** **Chair: TBA**	**Session P3: Layout Algorithms** **Chair: TBA**
4:00 PM to 4.30 PM	**Suryanarayana Adiga** and Vinay Shenoy, Philips Semiconductors, India. *Rapid System Prototyping*.	**Sreedhar Natarajan**, Texas Instruments Inc., Dallas, USA. *Memory Design Techniques. Invited Tutorial.*	**Jwalant Joshipura** ST Microelectronics, Noida, India**.** *Low-power Standard Cell Library Development*.
4.30 PM to 5.00 PM	**P. Wikneswaran**, CGoreEl, India. *Designing Multi-million gate FPGAs*		**Kamran Nabi Khan,** Controlnet India, Goa**.** *Alternate Flow to counter Antenna Problem in ASICs.*
5.00 PM to 5.30 PM			Sabyasachi Das, Intel Corporation, USA, and **Sunil P. Khatri**, University of Colorado, Boulder. *A Routing Technique for Structured Designs which Exploits Regularity. Invited talk.*
5.30 PM to 6.00 PM			Parthasartathi Dasgupta, IIM Calcutta. *TABULA: A Tabu-Search based Floorplan Area and Delay Optimizer*.
6.00 PM	*End of Day 1*		



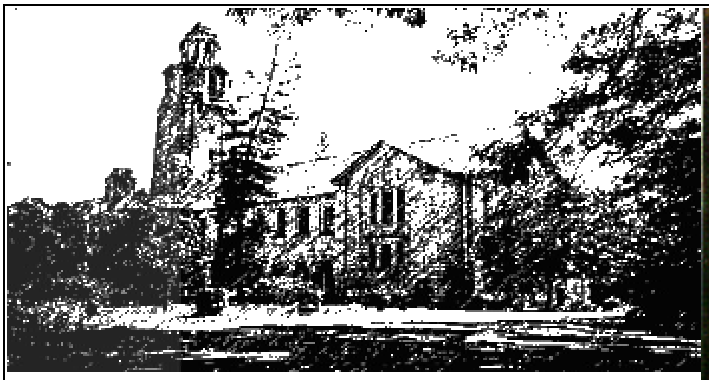




Advance Program for August 18, 2001 (Saturday)

Time	***Test Workshop*** ***Room: A***	***High-level and Logic Design Workshop*** ***Room: Main Auditorium***	***Physical Design and VLSI Technology Workshop*** ***Room: B***
	Session T3: Test Generation **Chair: TBA**	**Session L6: Low Power Design** **Chair: TBA**	**Session P4: Deep Submicron I** **Chair: TBA**
9:00 AM to 9:30 AM	**M.C. Bhuvaneshwari**, S. N. Sivanandan, Deno Mathew, G. Sundramurthi, PSG College, Coimbatore, India. *Parallel Guided Genetic Algorithm based Test pattern Generator using Message.*		P. R. Suresh and **Vipul Singhal**, Texas Instruments, India. *Technology Entitlement In Submicron Era. Invited Talk*.
9.30 AM to 10.00 AM	Ragahvendra Kulkarni, IIT Delhi, **Rajiv Nadig,** Analog Devices, India, Vivek Agarwal, IIT Delhi, and C.P. Ravikumar, Controlnet, India**.** *Functional Test Generation of a Pipelined Implementation of DLX Processor*.	**Kaushik Roy**, Purdue University, USA. *Low Power VLSI Design. Invited Tutorial.*	
10.00 AM to 10.30 AM	**Santanu Chattopadhyay,** IIT Guwahati**.** *Reordering Test Patterns with Don't Cares for minimizing power during Combinational Testing.*		**Partha Chakrabarti**, M. C. Gupta, P. K. Tiwari and V. Kumar, Institute of Technology, Banaras Hindu University. *A Two-Dimensional Simulator For Studying Ionizing Radiation Effects In Deep-Submicron MOSFETs.*
10.30 AM to 11.00 AM	Ravindra Saraf, IIT Bombay, **Rubin A Parekhji,** Texas Instruments India, and Arun N. Chandorkar, IIT Bombay. *Architecture for Programmable Memory BIST.*		
11:00 to 11:30 AM	*Tea Break*		
	Session T4: Testing II **Chair: TBA** **(Venue: Room A)**	**Session L7: System-level Design I** **Chair: TBA** **(Venue: Main Auditorium)**	
11:30 to 12:00 Noon	**Vishwani Agrawal**, Agere Systems, USA, Yong C. Kim, U. of Wisconsin, Madison, and K.K. Saluja, U. of Wisconsin, Madison. *Partial Scan Design With Guaranteed Combinational ATPG.*	**Amey Hegde**, Controlnet India, Goa. *A Comparison of USB and Firewire*.	
12:00 to 12:30PM	K. Nikila, Jais Abraham and **Rubin A Parekhji**, Texas Instruments India. Design *Tradeoffs in Logic BIST.*	**Nirav Patel** and G. N. Nandakumar, Agere Systems, India. *A Hierarchical Approach for Detecting Naming Incompatibilities in Design Database.*	
12:30 to 1:00 PM	**H. Rahman,** A.P.C. Roy Polytechnic, Calcutta, D. Das, Jadavpur University, and B. Bhattacharya, ISI Calcutta. *A testable design for detection of path delay faults using DSTL Array.*	**Rajeshwari Banakar**, Ranjan Bose, and M. Balakrishnan, IIT, Delhi**.** *Low Power Design: Abstraction Levels and RT Level Design Techniques.*	

1:00 to 2:00 PM	*Lunch*





The picture shows Jamsetji Nusserwanji Tata (1839-1904) who envisaged the Indian Institute of Science to promote original investigations in all branches of learning and to utilise them for the benefit of India. The sketch shows the main building of IISc. The statue of Late J.N. Tata in front of the main building is an awe-inspiring historical landmark.

	Session T5: SOC Testing **Chair:TBA**	**Session L8: System-level Design II** **Chair: TBA**	**Session P5: Deep Submicron II** **Chair: TBA**
2.00 to 2.30 PM	**David Khanna** and R. Madhu. Texas Instruments, India. *Telecom System-On-Chip Testing.*	**Shampa Chakraverty,** NSIT, New Delhi and C.P. Ravikumar, Controlnet (India). *A stochastic scheduling algorithm for Real-time Systems.*	**Vipul Singhal**, K.G. Sumanth, C.B. Keshav, and P.R. Suresh, Texas Instruments India. *Transitor Flaring in Deep submicron Manufacturing: Issues and Solutions.*
2.30 to 3.00 PM	**Surendra Batukdeo**, Mentor Graphics, Singapore. *DFT methodology*.	**Suteekshn Kumar**, Infineon Technologies India, Bangalore. *Fuzzy Sets for IP Core Compliance Levels.*	Navakant Bhat and **H. C. Srinivasaiah**, IISc Bangalore. *Optimization of 0.1 nm transistor using Disposable Spacer Technique*.
3.00 to 3.30 PM	**B. Suresh,** Vinod Menezes, Phani Kumar, and George Smolinski, Texas Instruments India. *Test Strategy for Next Generation System on Chip (SOC): Case Study Ethernet*.	**R. Raghuraman**, Texas Instruments, India. *EDA software - Where quality is not a wish but a must!!*	**S.C. Bose**, V. Sunitha, Chandra Shekhar, CEERI, Pilani, *Design Synthesis Of CMOS Operational Amplifier From User Specification*.
3.30 to 4.00 PM	*Tea*		
4.00 PM to 6.00 PM	**Session L9** **Panel Discussion: EDA and Design: Who is in the Driver's Seat?** **Moderator: C.P. Ravikumar** Panel: TBA		







Registration Information:
Registration permits you to participate in all the technical sessions and tutorials organized as part of the workshops. Refreshments and lunch will be provided to all registrants at no extra charge. Please send your registration fee through a draft made out to *VLSI Design and Test Workshops, 2001*. ***Make the draft payable at Canara Bank, IISc, Bangalore Branch.*** The draft must be sent to **Prof. Navakant Bhat, Department of Electronics and Communication Engineering, Indian Institute of Science, Bangalore, 560 012**, India. If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments. The current exchange rate is approximately 1 US dollar = 45 Indian rupees.

Registration Fees Before July 20, 2001

	Indian Participant	Foreign Participant
Academic Institution	Rs. 2000	USD. 50
Non-academic Institution	Rs. 5000	USD. 150

Registration Fees After July 20, 2001

	Indian Participant	Foreign Participant
Academic Institution	Rs. 2500	USD. 75
Non-academic Institution	Rs. 6000	USD. 175

Venue Information: The JN Tata Auditorium is located in the National Science Seminar Complex of the Indian Institute of Science, popularly known as the "Tata Institute." The institute is located close to Yashavantapuram and Malleshwaram. If you are going to take a Taxi or an Autorickshaw, ask the driver to take you to the *Tata Institute*. There is a separate gate to enter the JN Tata Auditorium.

- More information about the Indian Institute of Science is available from http://iisc.ernet.in.
- A map of IISc is available from http://cm.bell-labs.com/cm/cs/who/va/ (Look for Conference Site)
- Some useful websites which provide information on hotels and tourism in Bangalore are: http://www.geocities.com/Athens/2960/ www.bangalorehotels.net/ http://www.virtualbangalore.com/Tou/index.php3

Weather Information: The weather in Bangalore during August is pleasant (temperatures ranging in 25 degrees to 30 degrees centigrade), with intermittent rain.

Contact Information Please contact C.P. Ravikumar (cpravikumar@rediffmail.com) for clarifications.

Fellowships: A small number of full or partial waivers of registration fee are available for Indian students and Indian faculty. Preference will be given to attendees who request for partial waiver. Write to the organizing chair with a statement of purpose for attending the workshops before July 1, 2001. Please note that travel support and staying arrangements have to be made by the participant availing free registration.

Related Event: International Conference on VLSI Design, Bangalore, 2002: http://vlsi.ccrl.nj.nec.com/





Technical Program Committee

Program Chairs for the Workshops

High-level Design Workshop
Anshul Kumar, IIT Delhi

Physical Design Workshop
B. Bhattacharya, ISI Calcutta

Test Workshop
C.P. Ravikumar, Controlnet India

Members of Program Committee

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Susmita Sur-Kolay, ISI Calcutta, India
Alok Singh, Virage Logic, India

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